CS-200 – Computer Architecture
Fall 2024

Week		Date	Time	Room	Lecture	Lab	Deadline
1	Mon	09.09.24	1pm - 3pm	INF1 - INF3		Introduction to the infrastructure	**Monday 09.09: Lab A (published)**
	Wed	11.09.24	10am - noon	SG1	Introduction + 1a. Instruction Set Architecture (ISA Reminder, Assembly Language, Compilers)		
	Wed	11.09.24	1pm - 3pm	INF1 - INF3		**No labs**	
	Fri	13.09.24	10am - noon	STCC C	1b. Instruction Set Architecture (Branches, Functions, and Stack)		
2	Mon	16.09.24			**Holiday**		
	Wed	18.09.24	10am - noon	SG1	1c. Instruction Set Architecture (Memory and Addressing Modes)		
	Wed	18.09.24	1pm - 3pm	INF1 - INF3		Lab A (Game of Life)	
	Fri	20.09.24	10am - noon	**BCH 2201**	1c. Instruction Set Architecture (Memory and Addressing Modes; cont'd) + 1d. Instruction Set Architecture (Arrays and Data Structures)		
3	Mon	23.09.24	1pm - 3pm	INF1 - INF3		Lab A (Game of Life)	
	Wed	25.09.24	10am - noon	SG1	1e. Instruction Set Architecture (Arithmetic)		
	Wed	25.09.24	1pm - 3pm	INF1 - INF3		Exercises on Processors & ISA	
	Fri	27.09.24	10am - noon	STCC C	1e. Instruction Set Architecture (Arithmetic; cont'd) + 2a. Processor, I/Os, and Exceptions (Multicycle Processor)		
4	Mon	30.09.24	1pm - 3pm	INF1 - INF3		Lab A (Game of Life)	
	Wed	02.10.24	10am - noon	SG1	2a. Processor, I/Os, and Exceptions (Multicycle Processor; cont'd) + 2b. Processor, I/Os, and Exceptions (Inputs and Outputs)		
	Wed	02.10.24	1pm - 3pm	INF1 - INF3		Lab A (Game of Life)	
	Fri	04.10.24	10am - noon	**BCH 2201**	2b. Processor, I/Os, and Exceptions (Inputs and Outputs; cont'd) + 2c. Processor, I/Os, and Exceptions (Interrupts)		
5	Mon	07.10.24	1pm - 3pm	INF1 - INF3		Lab A (Game of Life)	
	Wed	09.10.24	10am - noon	SG1	2d. Processor, I/Os, and Exceptions (Exceptions)		
	Wed	09.10.24	1pm - 3pm	INF1 - INF3		Lab A (Game of Life)	
	Fri	11.10.24	10am - noon	**BCH 2201**	2d. Processor, I/Os, and Exceptions (Exceptions; cont'd) + 2e. Processor, I/Os, and Exceptions (An Example of I/Os and Exceptions)		**Sunday 13.10 @ 23:59: Lab A (final)**
6	Mon	14.10.24	1pm - 3pm	INF1 - INF3		Exercises on I/Os and Exceptions	**Monday 14.10: Lab B (published)**
	Wed	16.10.24	10am - noon	SG1	3a. Memory Hierarchy (Caches)		
	Wed	16.10.24	1pm - 3pm	INF1 - INF3		Lab B.1 (RISC-V Multicycle Processor): ALU	
	Fri	18.10.24			**No lecture**		
7	Mon	28.10.24	1pm - 3pm	INF1 - INF3		Lab B.2 (RISC-V Multicycle Processor): Core	
	Wed	30.10.24	10am - noon	SG1	3a. Memory Hierarchy (Caches; cont'd)		
	Wed	30.10.24	1pm - 3pm	INF1 - INF3		Lab B.2 (RISC-V Multicycle Processor): Core	
	Fri	01.11.24	10am - noon	STCC C	3b. Memory Hierarchy (Simple Cache Examples) + 3c. Memory Hierarchy (Virtual Memory)		**Sunday 03.11 @ 23:59: Lab B.1 (partial)**
8	Mon	04.11.24	1pm - 3pm	INF1 - INF3		Lab B.2 (RISC-V Multicycle Processor): Core	
	Wed	06.11.24	10am - noon	SG1	3c. Memory Hierarchy (Virtual Memory; cont'd) + 3d. Memory Hierarchy (Simple Virtual Memory Examples)		
	Wed	06.11.24	1pm - 3pm	INF1 - INF3		Exercises on Memory Hierarchy	
	Fri	08.11.24	10am - noon	STCC C	4a. Instruction-Level Parallelism (Performance) + 4b. Instruction-Level Parallelism (Basic Pipelining)		
9	Mon	11.11.24	1pm - 3pm	INF1 - INF3		Lab B.3 (RISC-V Multicycle Processor): Memory, Peripherals, and Integration	
	Wed	13.11.24	**10am - 1:15pm**	**TBA**	**Midterm**		
	Wed	13.11.24					
	Fri	15.11.24	10am - noon	STCC C	4c. Instruction-Level Parallelism (Pipelining)		
10	Mon	18.11.24	1pm - 3pm	INF1 - INF3		Lab B.3 (RISC-V Multicycle Processor): Memory, Peripherals, and Integration	
	Wed	20.11.24	10am - noon	SG1	4c. Instruction-Level Parallelism (Pipelining; cont'd)		
	Wed	20.11.24	1pm - 3pm	INF1 - INF3		Lab B.3 (RISC-V Multicycle Processor): Memory, Peripherals, and Integration	
	Fri	22.11.24	10am - noon	STCC C	4d. Instruction-Level Parallelism (Dynamic Scheduling)		**Sunday 24.11 @ 23:59: Lab B.2 (partial)**
11	Mon	25.11.24	1pm - 3pm	INF1 - INF3		Lab B.3 (RISC-V Multicycle Processor): Memory, Peripherals, and Integration	**Monday 25.11: Lab C (published)**
	Wed	27.11.24	10am - noon	SG1	4d. Instruction-Level Parallelism (Dynamic Scheduling; cont'd) + 4e. Instruction-Level Parallelism (Examples of Scheduling)		
	Wed	27.11.24	1pm - 3pm	INF1 - INF3		Lab C.1 (RISC-V Interrupts): Adding Interrupt Support	
	Fri	29.11.24	10am - noon	STCC C	4e. Instruction-Level Parallelism (Examples of Scheduling; cont'd) + 4f. Instruction-Level Parallelism (Besides and Beyond Superscalars)		**Sunday 01.12 @ 23:59: Lab B (final)**
12	Mon	02.12.24	1pm - 3pm	INF1 - INF3		Lab C.1 (RISC-V Interrupts): Adding Interrupt Support	
	Wed	04.12.24	10am - noon	SG1	4f. Instruction-Level Parallelism (Besides and Beyond Superscalars; cont'd)		
	Wed	04.12.24	1pm - 3pm	INF1 - INF3		Exercises on Instruction-Level Parallelism	
	Fri	06.12.24	10am - noon	STCC C	4f. Instruction-Level Parallelism (Besides and Beyond Superscalars; cont'd) + 4g. Instruction-Level Parallelism (Intel x86 and ARM)		
13	Mon	09.12.24	1pm - 3pm	INF1 - INF3		Lab C.2 (RISC-V Interrupts): Interrupt Controller and Integration	
	Wed	11.12.24	10am - noon	SG1	5a. Multiprocessors (Cache Coherence)		
	Wed	11.12.24	1pm - 3pm	INF1 - INF3		Lab C.2 (RISC-V Interrupts): Interrupt Controller and Integration	
	Fri	13.12.24	10am - noon	STCC C	5a. Multiprocessors (Cache Coherence; cont'd) + 5b. Multiprocessors (Examples of Cache Coherence)		**Sunday 15.12 @ 23:59: Lab C.1 (partial)**
14	Mon	16.12.24	1pm - 3pm	INF1 - INF3		Lab C.2 (RISC-V Interrupts): Interrupt Controller and Integration	
	Wed	18.12.24	10am - noon	SG1	5c. Multiprocessors (Memory Consistency)		
	Wed	18.12.24	1pm - 3pm	INF1 - INF3		Exercises on Multiprocessors	
	Fri	20.12.24	10am - noon	STCC C	6. Hardware Security		**Sunday 22.12 @ 23:59: Lab C (final)**